

FEATURES

Guaranteed Monotonic Over Temperature
Unipolar Or Bipolar Operation
Buffered Voltage Outputs
High-Speed Serial Digital Interface
Reset to Zero- Or Center-Scale
Wide Supply Range, +5V-Only to $\pm 15V$
Low Power Consumption (60mW max)
Available In 16-pin DIP and SO Packages

APPLICATIONS

Software-Controlled Calibration
Servo Controls
Process Control and Automation

GENERAL DESCRIPTION

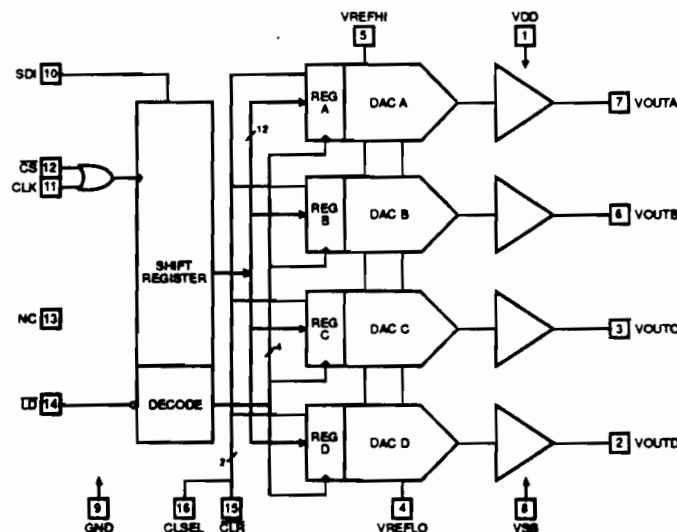
The DAC-8420 is a quad, 12-bit voltage-output DAC with serial digital interface, in a 16-pin package. Utilizing BiCMOS technology, this monolithic device features unusually high circuit density and low power consumption. The simple, easy-to-use serial digital input and fully buffered analog voltage outputs require no external components to achieve specified performance.

The three-wire serial digital input is easily interfaced to microprocessors running up to 20MHz clock rates, with minimal additional circuitry. Each DAC is addressed individually by a 16-bit serial word consisting of a 12-bit data word with an address header. The user-programmable reset control CLR forces all four DAC outputs to either zero- or midscale, asynchronously overriding the current DAC register values. The output voltage range, determined by the inputs VREFH and VREFLO, is set by the user for positive or negative Unipolar or Bipolar signal swings within the supplies. This structure allows considerable design flexibility, yielding circuits with low temperature drift.

The DAC-8420 is available in 16-pin epoxy DIP, CerDIP, and wide-body SO (small-outline surface mount) packages. Operation is specified with supplies ranging from +5V-only to $\pm 15V$, with references of +2.5V to $\pm 10V$ respectively. Power dissipation when operation from $\pm 15V$ supplies is less than 330mW(max), and only 60mW(max) with a +5V supply.

For applications requiring product meeting MIL-STD-883, contact your local sales office for the DAC-8420/883 data sheet, which specifies operation over the $-55^{\circ}C$ to $+125^{\circ}C$ temperature range.

FUNCTIONAL DIAGRAM



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DAC-8420

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DAC-8420– SPECIFICATIONS

ELECTRICAL CHARACTERISTICS at $V_{DD}=+5.0V \pm 5\%$, $V_{SS}=0.0V$, $V_{REFH}=+2.5V$, $V_{REFL}=0.0V$, and $V_{SS} = -5.0V \pm 5\%$, $V_{REFL}=-2.5V$. $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ unless otherwise specified. See Note 1 for supply variations.

| PARAMETER | COND | MIN | TYP | MAX | UNITS |
|------------------------|------|-----------------------|-----|---------|------------------|
| Integral Linearity "E" | INL | | .5 | ± 1 | LSB |
| Integral Linearity "E" | INL | Note 2, $V_{SS} = 0V$ | | ± 2 | LSB |
| Integral Linearity "F" | INL | | | ± 2 | LSB |
| Integral Linearity "F" | INL | Note 2, $V_{SS} = 0V$ | | ± 4 | LSB |
| Differential Linearity | DNL | Monotonic over temp. | -1 | | LSB |
| Min Scale Error | ZSE | | | ± 4 | LSB |
| Full Scale Error | FSE | | | ± 4 | LSB |
| Min Scale Error | ZSE | Note 2, $V_{SS} = 0V$ | | ± 8 | LSB |
| Full Scale Error | FSE | Note 2, $V_{SS} = 0V$ | | ± 8 | LSB |
| Min Scale Tempco | | | 100 | | ppm/ $^{\circ}C$ |
| Full Scale Tempco | | | 100 | | ppm/ $^{\circ}C$ |

MATCHING PERFORMANCE

| | | | | | |
|--------------------|--|--|---------|--|-----|
| Linearity Matching | | | ± 1 | | LSB |
|--------------------|--|--|---------|--|-----|

REFERENCE

| | | | | |
|--------------------------------|-----------------------|-----------------------|----------------|---------|
| Positive Reference Input Range | Note 2 | $V_{REFL}+2.5$ | $V_{DD}-2.5$ | V |
| Negative Reference Input Range | Note 2 | V_{SS} | $V_{REFH}-2.5$ | V |
| Negative Reference Input Range | Note 2, $V_{SS} = 0V$ | 0 | $V_{REFH}-2.5$ | V |
| Reference High Input Current | I_{REFH} | Code 000 _H | 0 | +1.0 mA |

AMPLIFIER CHARACTERISTICS

| | | | | | |
|----------------|-----------|------------|-------|-------|--------------|
| Output Current | I_{OUT} | | -1.25 | +1.25 | mA |
| Settling Time | t_s | to .01% | 6 | | μsec |
| Slew Rate | SR | 10% to 90% | 2.2 | | V/ μsec |

LOGIC CHARACTERISTICS

| | | | | | |
|--------------------------|-----------|----------------------|-----|-----|---------|
| Logic Input High Voltage | V_{INH} | $T_A = +25^{\circ}C$ | 2.4 | | V |
| Logic Input Low Voltage | V_{INL} | $T_A = +25^{\circ}C$ | | 0.8 | V |
| Logic Input Current | I_{IN} | | | 1 | μA |
| Input Capacitance | C_{IN} | | 8 | | pF |

LOGIC TIMING CHARACTERISTICS (Note 3)

| | | | | | |
|------------------------|-----------|--|----|--|----|
| Data Setup Time | t_{ds} | | | | ns |
| Data Hold | t_{dh} | | | | ns |
| Clock Pulse Width HIGH | t_{ch} | | 60 | | ns |
| Clock Pulse Width LOW | t_{cl} | | 60 | | ns |
| Select Time | t_{css} | | | | ns |
| Deselect Delay | t_{csh} | | | | ns |
| Load Disable Time | t_{ld1} | | | | ns |
| Load Delay | t_{ld2} | | | | ns |
| Load Pulse Width | t_{ldw} | | | | ns |
| Clear Pulse Width | t_{clr} | | | | ns |
| Settling Time | t_s | | | | ns |

SUPPLY CHARACTERISTICS

| | | | | | |
|--------------------------|------------|--|-----|----|-------|
| Power Supply Sensitivity | PSS | | 100 | | ppm/V |
| Positive Supply Current | I_{DD} | | 7 | 12 | mA |
| Negative Supply Current | I_{SS} | | -10 | -7 | mA |
| Power Dissipation | P_{DISS} | | | 60 | mW |

NOTES:

1. All supplies can be varied $\pm 5\%$ and operation is guaranteed. Device is tested with $V_{DD}=+4.75V$.
2. Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
3. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of 1.6V.

DAC-8420 – ±15 Volt Specifications

ELECTRICAL CHARACTERISTICS at $V_{DD}=+15.0V$, $V_{SS}=-15.0V$, $V_{REFH}=+10.0V$, $V_{REFL}=-10.0V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ unless otherwise specified. See Note 1 for supply variations.

| PARAMETER | COND | MIN | TYP | MAX | UNITS |
|------------------------|-------|----------------------------|-----|-----|--------|
| Integral Linearity "E" | INL | | .25 | ±.5 | LSB |
| Integral Linearity "F" | INL | | | ±1 | LSB |
| Differential Linearity | DNL | Monotonic Over Temperature | -1 | | LSB |
| Min Scale Error | ZSE | $R_L = 2k\Omega$ | | ±2 | LSB |
| Full Scale Error | FSE | $R_L = 2k\Omega$ | | ±2 | LSB |
| Min Scale Tempco | TCZSE | $R_L = 2k\Omega$ | 15 | | ppm/°C |
| Full Scale Tempco | TCFSE | $R_L = 2k\Omega$ | 20 | | ppm/°C |

MATCHING PERFORMANCE

| | | | | | |
|--------------------|--|--|----|--|-----|
| Linearity Matching | | | ±1 | | LSB |
|--------------------|--|--|----|--|-----|

REFERENCE

| | | | | | |
|--------------------------------|--------|----------------|--|----------------|---|
| Positive Reference Input Range | Note 2 | $V_{REFL}+2.5$ | | $V_{DD}-2.5$ | V |
| Negative Reference Input Range | Note 2 | -10 | | $V_{REFH}-2.5$ | V |

| | | | | | |
|------------------------------|------------|-------|------|-------|----|
| Reference High Input Current | I_{REFH} | -2.75 | +1.5 | +2.75 | mA |
| Reference Low Input Current | I_{REFL} | -2.75 | -2 | 0 | mA |

AMPLIFIER CHARACTERISTICS

| | | | | | |
|----------------|-----------|------------|-----|----|--------|
| Output Current | I_{OUT} | -5 | | +5 | mA |
| Settling Time | t_s | to .01% | 8 | | μsec |
| Slew Rate | SR | 10% to 90% | 2.3 | | V/μsec |

LOGIC CHARACTERISTICS

| | | | | | |
|--------------------------|-----------|----------------------------------|-----|-----|-----|
| Logic Input High Voltage | V_{INH} | $T_A = +25^{\circ}C$ | 2.4 | | V |
| Logic Input Low Voltage | V_{INL} | $T_A = +25^{\circ}C$ | | 0.8 | V |
| Logic Input Current | I_{IN} | | | 1 | μA |
| Input Capacitance | C_{IN} | | 8 | | pF |
| Crosstalk | | | >72 | | dB |
| Large Signal Bandwidth | | -3dB, $V_{REFH} = 1$ to +10V typ | 160 | | kHz |

LOGIC TIMING CHARACTERISTICS (Note 3)

| | | | | | |
|------------------------|-----------|----|---|--|----|
| Data Setup Time | t_{ds} | 20 | | | ns |
| Data Hold | t_{dh} | 20 | | | ns |
| Clock Pulse Width HIGH | t_{ch} | 30 | | | ns |
| Clock Pulse Width LOW | t_{cl} | 50 | | | ns |
| Select Time | t_{css} | 50 | | | ns |
| Deselect Delay | t_{csh} | 10 | | | ns |
| Load Disable Time | t_{ld1} | 50 | | | ns |
| Load Delay | t_{ld2} | 10 | | | ns |
| Load Pulse Width | t_{ldw} | 40 | | | ns |
| Clear Pulse Width | t_{clr} | 50 | | | ns |
| Settling Time | t_s | | 6 | | μs |

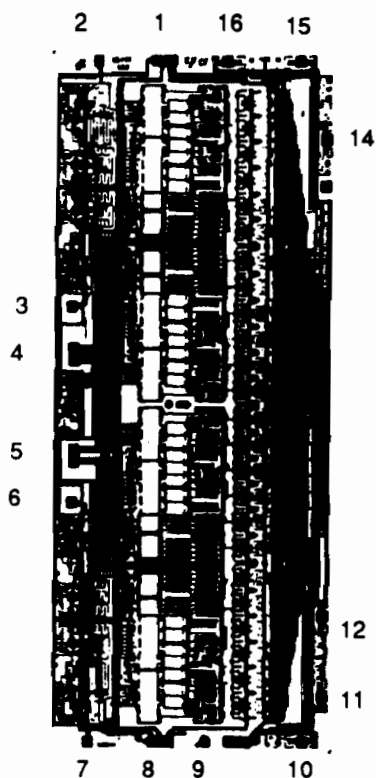
SUPPLY CHARACTERISTICS

| | | | | | |
|--------------------------|------------|--|-----|-----|-------|
| Power Supply Sensitivity | PSS | | | 150 | ppm/V |
| Positive Supply Current | I_{DD} | $V_{REFH} = +2.5V$, $V_{REFLO} = -2.5V$ | 7 | 12 | mA |
| Negative Supply Current | I_{SS} | | -10 | -7 | mA |
| Power Dissipation | P_{DISS} | | | 330 | mW |

NOTES:

1. All supplies can be varied ±5% and operation is guaranteed. Device is tested with nominal supplies.
2. Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
3. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of 1.6V.

DICE CHARACTERISTICS



- | | |
|-------------------|-----------|
| 1. VDD(Substrate) | 9. GND |
| 2. VOUTD | 10. SDI |
| 3. VOUTC | 11. CLK |
| 4. VREFLO | 12. CS\ |
| 5. VREFHI | 13. NC |
| 6. VOUTB | 14. LD\ |
| 7. VOUTA | 15. CLR\ |
| 8. VSS | 16. CLSEL |

DIE SIZE 0.119 X 0.283 inch, 33,677sq. mils
(3.023 X 7.188 mm, 21.73 sq. mm)

For additional DICE ordering information, refer to Data Book.

WAFER TEST LIMITS at $V_{DD} = +15.0\text{ V}$, $V_{SS} = -15.0\text{ V}$, $V_{REFHI} = +10.0\text{ V}$, $V_{REFLO} = -10.0\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise specified.

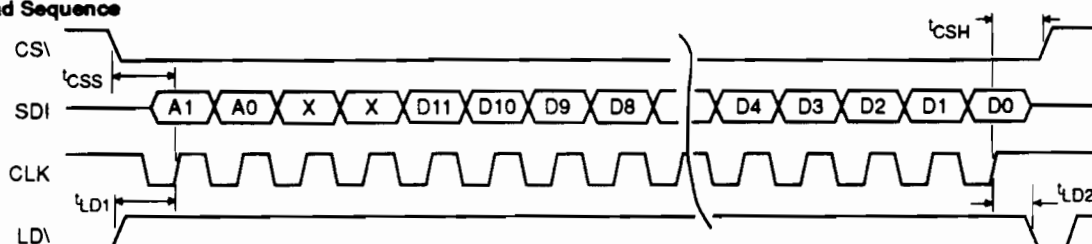
| PARAMETER | SYMBOL | CONDITIONS | DAC-8420G | |
|---------------------------|-----------|------------|-----------|-------------------|
| | | | LIMIT | UNITS |
| Integral Nonlinearity | INL | | ± 1 | LSB MAX |
| Differential Nonlinearity | DNL | | ± 1 | LSB MAX |
| Min Scale Offset | | | ± 1 | LSB MAX |
| Max Scale Offset | | | ± 1 | LSB MAX |
| Logic Input High Voltage | V_{INH} | | 2.4 | V MIN |
| Logic Input Low Voltage | V_{INL} | | 0.8 | V MAX |
| Logic Input Current | I_{IN} | | 1 | μA MAX |
| Positive Supply Current | I_{DD} | | 15 | mA MAX |
| Negative Supply Current | I_{SS} | | 10 | mA MAX |

NOTE:

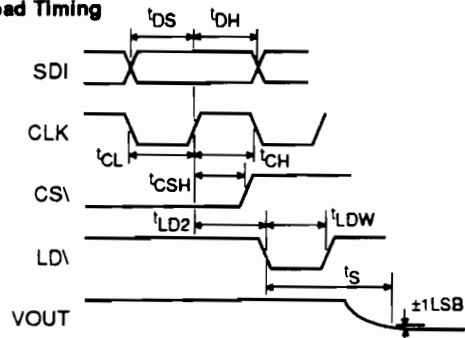
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TIMING DIAGRAM

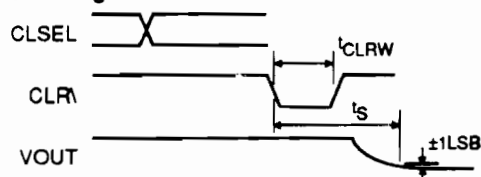
Data Load Sequence



Data Load Timing



Clear Timing



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| | |
|---------------------------------------|----------------------------------|
| V_{SS} to V_{DD} | -0.3 V, +36.0 V |
| V_{SS} to GND | -0.3 V, +18.0V |
| V_{DD} to GND | +0.3 V, -18.0 V |
| V_{SS} to VREFLO | -0.3 V, $V_{SS} - 2.0\text{V}$ |
| VREFHI to VREFLO | +2.0 V, $V_{SS} - V_{DD}$ |
| VREFHI to V_{DD} | +2.0 V, +33.0V |
| IREFHI, IREFLO | ? mA |
| Current into Any Pin | ± 15 mA |
| Digital Input Voltage to DGND | -0.3V, $V_{LOGIC} + 0.3\text{V}$ |
| Operating Temperature Range | |
| EP, FP, ES, FS, ET, FT | -40°C to +85°C |
| BT | -55°C to +125°C |
| Dice Junction Temperature | +150°C |
| Storage Temperature | -65°C to +150°C |
| Power Dissipation | 1000mW |
| Lead Temperature (Soldering, 60 sec.) | 300°C |

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket.

| PACKAGE TYPE | Thermal Resistance | |
|---|--------------------|---------------|
| | Θ_{JA}^1 | Θ_{JC} |
| | UNITS | |
| 16-Pin Plastic DIP (P) | xx | xx |
| | °C/W | |
| 16-Pin Hermetic DIP (T) | xx | xx |
| | °C/W | |
| 16-Lead Small Outline Surface Mount (S) | xx | xx |
| | °C/W | |

NOTE:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep unit conductive foam or packaging at all times until ready to use. Use proper anti-static handling procedures.
3. Remove power before inserting or removing units from their sockets.
4. Analog Outputs are protected from short circuits to ground or either supply.

CAUTION:

PIN FUNCTION DESCRIPTION

POWER SUPPLIES

VDD: Positive Supply, +5V to +15V.

VSS: Negative Supply, 0 to -15V.

GND: Digital Ground.

CLOCK

CLK: System Serial Data Clock Input, TTL/CMOS levels. Data presented to the input SDI on the falling edge of clock is shifted into the internal serial-parallel input register. This input is logically ANDed with CS\.

CONTROL INPUTS (All are CMOS/TTL compatible)

CLR\: Asynchronous Clear, active low. Sets internal data registers A - D to zero or mid-scale, depending on current state of CLSEL. The data in the serial input shift register is unaffected by this control.

CLSEL: Determines action of CLR\. If HIGH, a Clear command will set the internal DAC registers A - D to mid-scale (800_H). If LOW, the registers are set to zero (000_H).

CS\: Device Chip Select, active low. This input is logically ANDed with the clock and disables the serial data register input when HIGH. When LOW, data input clocking is enabled. See the Control Function Table.

LD\: Asynchronous DAC Register Load Control, active low. The data currently contained in the serial input shift register is shifted out to the DAC data registers on the falling edge of LD\, independent of CS\. Input data must remain stable while LD\ is LOW.

DATA INPUT (All are CMOS/TTL compatible)

SDI: Serial Data Input. Data presented to this pin is loaded into the internal serial-parallel shift register, which shifts data in beginning with DAC address bit A1. This input is ignored when CS\ is HIGH.

The format of the 16-bit serial word is:

| (FIRST) | | | | | | | | | | | | | | | | | (LAST) |
|------------------|----|----|----|-------|-----------------------|----|----|----|----|-----|-----|-----|-----|-----|-----|--|--------|
| B0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | B9 | B10 | B11 | B12 | B13 | B14 | B15 | | |
| A1 | A0 | NC | NC | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| - Address Word - | | | | (MSB) | --- DAC Data Word --- | | | | | | | | | | | | (LSB) |

REFERENCE INPUTS

VREFHI: Upper DAC ladder reference voltage input. Allowable range is (VDD-2.5V) to (VREFLO+2.5V).

VREFLO: Lower DAC ladder reference voltage input, equal to zero scale output. Allowable range is VSS to (VREFHI-2.5V).

ANALOG OUTPUTS

VOUTA through VOUTD: Four buffered DAC voltage outputs.

CONTROL FUNCTION TABLE

| CLK ¹ | CS ¹ | LD\ | CLR\ | CLSEL | Serial Input Shift Register | DAC Registers A- D |
|------------------|-----------------|-----|------|-------|-----------------------------|---|
| NC | H | H | L | H | No Change | Loads midscale value (40 _H) |
| NC | H | H | L | L | No Change | Loads zero scale value (00 _H) |
| NC | H | H | ↑ | H/L | No Change | Latches value |
| ↓ | L | H | H | NC | Reads in serial input SDI | No Change |
| ↑ | L | H | H | NC | Shifts register one bit. | No Change |
| H | NC (↑) | ↓ | H | NC | No Change | Loads the serial data word ² |
| H | NC | L | H | NC | No Change | Transparent ³ |
| NC | H | H | H | NC | No Change | No Change |

NC = Don't Care.

Notes

1. CS\ and CLK are interchangeable.

2. Returning CS\ HIGH while CLK is HIGH avoids an additional "false clock" of serial input data. See Note 1.

3. Do not clock in serial data while LD\ is LOW.

DIGITAL INTERFACE OPERATION

The serial input of the DAC-8420, consisting of CS\, SDI, and LD\, is easily interfaced to a wide variety of microprocessor serial ports. As shown in the Control Function Table and the Timing Diagram, while CS\ is LOW the data presented to the input SDI is shifted into the internal serial/parallel shift register on the rising edge of the clock, with the address MSB first, data LSB last. The data format, shown above, is two bits of DAC address and two "don't care" fill bits, followed by the 12-bit DAC data word. Once all 16 bits of the serial data word have been input, the load control LD\ is strobed and the word is parallel-shifted out onto the internal data bus. The two address bits are decoded and used to route the 12-bit data word to the appropriate DAC data register.

DAC ADDRESS WORD DECODE TABLE

| A1 | A0 | DAC Addressed |
|----|----|---------------|
| 0 | 0 | DAC A |
| 0 | 1 | DAC B |
| 1 | 0 | DAC C |
| 1 | 1 | DAC D |

ANALOG OUTPUT CODE TABLE

| DAC Data Word (HEX) | VOUT | Note |
|---------------------|---|-------------------|
| FFF | $VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 4095$ | Full-scale output |
| 801 | $VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2049$ | Midscale + 1 |
| 800 | $VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2048$ | Midscale |
| 7FF | $VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2047$ | Midscale - 1 |
| 000 | $VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 0$ | Zero-scale |

PROGRAMMING THE ANALOG OUTPUTS

The unique differential reference structure of the DAC-8420 allows the user to tailor the output voltage range precisely to the needs of the application. Instead of wasting DAC resolution on an unused region near the positive or negative rail, the DAC-8420 allows the user to determine both the upper and lower limits of the analog output voltage range. Thus, as shown in the Analog Output Code Table the outputs of DACs A through D range between VREFHI and VREFLO, within the limits specified in the Electrical Characteristics tables.

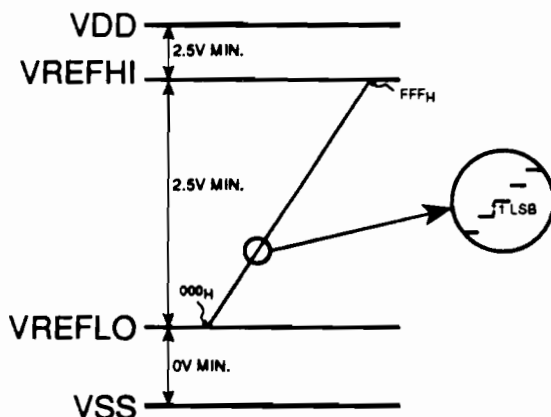
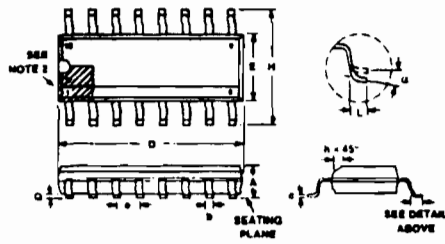


Figure X. Output Voltage Range Programming

PACKAGE DIMENSIONS

16-Pin Epoxy DIP (P)

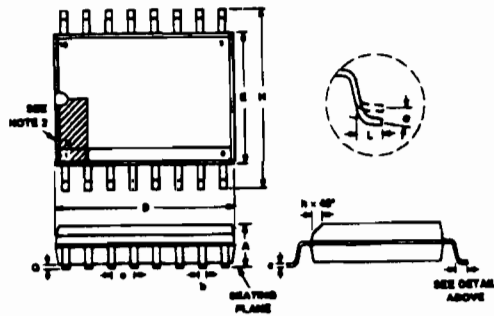


| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|------------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | |
| b | 0.0138 | 0.0182 | 0.35 | 0.49 | |
| c | 0.0075 | 0.0080 | 0.19 | 0.20 | |
| D | 0.3858 | 0.3837 | 9.80 | 10.00 | |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | |
| e | 0.0500 BSC | | 1.27 BSC | | |
| h | 0.0099 | 0.0198 | 0.25 | 0.50 | |
| L | 0.0160 | 0.0500 | 0.41 | 1.27 | |
| Q | 0.0040 | 0.0098 | 0.10 | 0.25 | |
| n | 0" | 8" | 0" | 8" | |

NOTES

1. Package dimensions conform to JEDEC specification MS-012-AC (Issue A, June 1985).
2. Index area; a dimple or lead end identification mark is located adjacent to lead one and is within the shaded area shown.

16-Pin SOIC (S)



| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|------------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0020 | 0.1040 | 2.30 | 2.65 | |
| b | 0.0138 | 0.0182 | 0.35 | 0.49 | |
| c | 0.0091 | 0.0135 | 0.23 | 0.34 | |
| D | 0.3077 | 0.4125 | 10.10 | 10.50 | |
| E | 0.2014 | 0.2882 | 7.40 | 7.80 | |
| H | 0.3097 | 0.4105 | 10.00 | 10.50 | |
| e | 0.0500 BSC | | 1.27 BSC | | |
| h | 0.0080 | 0.0291 | 0.25 | 0.74 | |
| L | 0.0167 | 0.0500 | 0.40 | 1.27 | |
| Q | 0.0040 | 0.0110 | 0.10 | 0.28 | |
| n | 0" | 8" | 0" | 8" | |

NOTES

1. Package dimensions conform to JEDEC specification MS-013-AA (Issue A, June 1985).
2. Index area; a dimple or lead end identification mark is located adjacent to lead one and is within the shaded area shown.